REMARKS

Claims 1-5 are pending in this application, of which claim 1 has been amended. No new claims have been added.

Claims 1-5 stand rejected under 35 USC § 112, second paragraph, as indefinite.

Accordingly, claim 1 has been amended to clarify that the gradually rising and gradually falling waveform for the power clock signal is a "non-rectangular" shape. Figs. 4-7 show the non-rectangular clock waveforms of the present invention, in contrast to the rectangular clock waveforms of the conventional prior art shown in Figs. 8-9.

Thus, the 35 USC §112, second paragraph, rejection should be withdrawn

Claims 1-3 and 5 stand rejected under 35 USC § 103(a) as unpatentable over **Ueda et al.** (previously applied) in view of "A Low Power Multiplier Using Adiabatic Charging Binary Decision Diagram Circuit", Shunji Nakata, Takakuni Douseki, and Yuichi Kado, 1999 International Conference on Solid State Devices and Materials, Tokyo, 1999, pp. 444-445, (hereinafter "**Nakata et al.**").

Applicants respectfully traverse this rejection.

As noted in Applicants' previous response of October 31, 2002, **Ueda et al.** discloses a flip-flop circuit constituted by two latch circuits of the same structure that are cascaded. Each latch circuit includes an inverter formed of a P channel transistor and an N channel transistor, an N channel transistor connected between a common node and a ground node, and two data input/output terminals. Two kinds of clock signals supplied to gates of N channel transistors are complementary to each other.

The Examiner has admitted that **Ueda et al.** does not disclose that a charge recycle power source is used to generate the clock signal, but has cited **Nakata et al.** for teaching this feature.

Applicants respectfully disagree. Although Fig.1 (b) of **Nakata et al.** shows non-rectangular power clock waveforms, as in the present invention, neither **Ueda et al.** nor **Nakata et al.** teaches, mentions or suggests satisfaction of the following inequality recited in claim 1 of the instant application:

$$|V_{TN}|+|V_{TP}| \geq VDD,$$

where V_{TN} is a threshold of the n-channel MOSFET transistor, V_{TP} is a threshold of the p-channel MOSFET, and VDD is an output voltage of the charge recycle power source.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-5, as amended, are in condition for further examination.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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